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EXAMINER	
VIGUSHIN, JOHN B	
ART UNIT	**PAPER NUMBER**
2827	

DATE MAILED: 12/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/964,151	BOYLAN ET AL.	
	Examiner	Art Unit	
	John B. Vigushin	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 August 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 13-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 13-15* is/are rejected.

7)☒ Claim(s) *16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The present Office Action is responsive to Applicant's Response filed August 11, 2003. The Examiner acknowledges the amendments to Claims 13 and 14, and the addition of new Claims 15 and 16. Accordingly, Claims 1-10 and 13-16 are now pending in the instant amended Application.

Rejections Based On Prior Art

2. The following references were relied upon for the rejections hereinbelow:

Iversen et al. (US 6,384,492 B1)* Patel et al. (US 6,366,467 B1)*

McDonnal (US 5,075,821)* Li (US 6,525,944 B1)*

*Previously made of record in the instant Application

Claim Rejections - 35 USC § 102/103

3. Claims 1-7, 9, 10, 13 and 15 are rejected under 35 U.S.C. 102(e) as anticipated by Patel et al. or, in the alternative, under 35 U.S.C. 103(a) as obvious over Patel et al. in view of Li.

Rejection #1 of Claim 1:

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-7, 9, 10, 13 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Patel et al.

As to Claim 1, Patel et al. discloses, in Fig. 5, an adapter (interposer) 506 comprising: a first (top) and a second (bottom) surface; at least one first interconnect, i.e., the pads, not shown, on the first surface of adapter 506 that receive and electrically connect the BGA bumps of carrier 502 to adapter 506; at least one second interconnect (pins 508; col.4: 62-66) on the second surface; since second interconnects 508 supply power to step down converter (SDC) 518 on carrier 502 (col.4: 66), then at least one connective path inherently exists between the first and second interconnects; a signal modifying circuit (comprising input capacitor 522 and input inductor 524) between the first interconnects and second interconnects 508, as disclosed in an alternate case of the Fig. 5 embodiment wherein said input capacitor 522 and input inductor 524 are mounted on the adapter 506, as in the embodiment of Fig. 3 (Fig. 3 and col.3: 63-64; Fig. 5 and col.5: 14-15); the second interconnects 508 are *pins* that are **used** as *socket connects* in Patel et al. (col.4: 62-66). However, since the Applicant **does not positively claim a structure such as a printed circuit board having through holes** (or, for that matter, a surface mounted socket structure) for receiving the pins, then the Applicant's recitation of "through hole connect" is nothing more than the recitation of a pin with an **intended use** (i.e., a pin *for connection to some unclaimed structure having a through hole*). Accordingly, the Examiner reads the limitation "through hole connect" as a pin which is met by any of the pins 508 of Patel et al. which may be used as a

socket connect (as, in fact, disclosed by Patel et al. in Fig. 5, socket 512) or as a *through hole connect* in a through hole structure, **neither** a socket **nor** a through hole structure being positively claimed by the Applicant and therefore **neither** socket **nor** through hole structure required to be met by the prior art. The Applicant's recitation "through hole connect" is merely a recitation of the **intended use** of a pin: It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. *Ex parte Masham*, 2 USPQ2d 1647 (1987).

Or, in the alternative, Rejection #2 of Claim 1:

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7, 9, 10, 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patel et al. in view of Li.

As to Claim 1:

I. Patel et al. discloses, in Fig. 5, an adapter (interposer) 506 comprising: a first (top) and a second (bottom) surface; at least one first interconnect, i.e., the pads, not shown, on the first surface of adapter 506 that receive and electrically connect the BGA bumps of carrier 502 to adapter 506; at least one second interconnect (pins 508; col.4: 62-66) on the second surface; since second interconnects 508 supply power to step

down converter (SDC) 518 on carrier 502 (col.4: 66), then at least one connective path inherently exists between the first and second interconnects; a signal modifying circuit (comprising input capacitor 522 and input inductor 524) between the first interconnects and second interconnects 508, as disclosed in an alternate case of the Fig. 5 embodiment wherein said input capacitor 522 and input inductor 524 are mounted on the adapter 506, as in the embodiment of Fig. 3 (Fig. 3 and col.3: 63-64; Fig. 5 and col.5: 14-15).

II. Patel et al. discloses that second interconnects 508 are pins which function as *socket connects* for insertion into socket 512 (col.4: 62-66). Patel et al. does not teach that second interconnects 508 are "through hole connects;" i.e., pins intended for use as pin connectors for direct insertion into the through holes of a printed circuit board or the through holes of some other circuit substrate.

III. Li discloses a package 400 comprising a die 430 mounted on an adapter (interposer) 412, said adapter having first (pad) interconnects on the top surface thereof that receive the solder balls 422, and second (pin) interconnects on the bottom surface thereof that function equivalently as socket connects in one embodiment (for insertion into a socket, not shown, that is surface mounted on a printed circuit board 440) and as through hole connects in another embodiment (for insertion directly into through holes of the printed circuit board as shown in Fig. 4) (col.4: 47-54). Thus, Li shows that the pin-receiving socket mounted on the printed circuit board 440, and the through-holes fabricated in the printed circuit board 440 itself are equivalent structures known in the

art for connecting a package 400 with through hole connects (i.e., pins 424) to a printed circuit board 440.

IV. Since Patel et al. and Li are both in the electronic packaging art requiring board adapters for mounting electronic devices onto a printed circuit board, and since Li discloses that the second (pin) interconnects can be inserted into a socket on a printed circuit board, or, alternatively, directly into the through holes of a printed circuit board--i.e., since the pin-receiving socket and the through-holes directly fabricated in the printed circuit board were shown to be art-recognized equivalents by Li at the time the invention was made--then one of ordinary skill in the art at the time the invention was made would have found it obvious to substitute the socket in Patel et al. with through-holes in the printed circuit board of Patel et al. for applications requiring reduction in weight and size of a package (to which sockets significantly contribute) and/or applications in environments prone to mechanical shock and vibrations which tend to loosen the component in the socket and resulting in electrical disconnect and causing the socket to be a source of circuit noise.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the assembly of Patel et al. by removing the socket 512 (and socket 514 as well) and directly connecting second (pin) interconnects 508 into the through holes of printed circuit board (PCB) 516 for applications that do not require or cannot support a socket (such as applications in an environment prone to mechanical shock and vibration) and further require a smaller, lighter packaging,

wherein the direct adapter-to-PCB connection eliminates the use of a socket which is a source of noise in the circuit.

As to Claim 2, Patel et al. further discloses that said first interconnects are physically spaced to correspond to a first pin configuration (i.e., BGA or PGA of carrier 502) of a power module, the power module comprising BGA carrier 502 and SDC 518 (Fig. 5; col.5: 6-8). Note that the BGA (ball grid array) of carrier (package) 502 is disclosed as a PGA (pin grid array) in an alternate embodiment (col.3: 40-42).

As to Claim 3, Patel et al. further discloses that the second interconnects 508 are physically spaced to correspond to a second pin configuration of an end user's circuit board 516 by way of the circuit board socket 512 (Fig. 5; col.4: 64-66) or by direct connection to the through holes of circuit board 516 in Patel et al. as modified, above, by Li (see Li, Fig. 4 and col.4: 46-54).

As to Claim 4, Patel et al. further discloses that a signal modifying circuit (i.e., input capacitor 522 and input inductor 524 mounted on adapter 506 in the alternative embodiment of Fig. 5, as indicated in col.5: 14-15) acts upon an input to the adapter 506 (just as in the embodiment of Fig. 3; col.3: 63-64).

As to Claim 5, Patel et al. further discloses that a signal modifying circuit (i.e., output capacitor 526 and output inductor 528 mounted on adapter 506; col.5: 11-12) acts upon an output to the adapter 506 (just as in the embodiment of Fig. 3; col.3: 64-65).

As to Claim 6, Patel et al. further discloses that the power module is a DC-to-DC converter (the DC power originates with a battery and a voltage regulator circuit provides a steady DC voltage having the correct amplitude; col.1: 11-16).

As to Claim 7, Patel et al. further discloses that the power module is an AC-to-DC converter (the DC power has been converted from AC power and a voltage regulator circuit provides a steady DC voltage having the correct amplitude; col.1: 11-16 and 29-32).

As to Claim 9, Patel et al. further discloses that, in the case where the first interconnects receive BGA bumps of the carrier 502 (col.3: 40-42), said first interconnects inherently comprise surface mount connects.

As to Claim 10, Patel et al. further discloses that, in the case where the first interconnects receive PGA pins of the carrier 502 (col.3: 40-42), said first interconnects inherently comprise through-hole connects.

As to Claim 13, Patel et al. further discloses that the signal modifying circuit–input capacitor 522 and input inductor 524 (col.5: 14-15)–comprises a filter; i.e., the signal modifying circuit filters the input power (just as in the Fig. 3 embodiment; col.3: 63-64).

As to Claim 15, Patel et al. further discloses, in Fig. 5: at least a second interconnect on the first surface, i.e., the pads, not shown, on the first surface of adapter 506 that receive and electrically connect the BGA bumps of carrier 504 to adapter 506; at least one connective path between the first interconnect on the first surface and the second interconnect on the first surface (col.5: 1-3); a signal modifying circuit (output

capacitor 526 and output inductor 528; col.5: 11-12) between the first interconnect on the first surface and the second interconnect on the first surface.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Patel et al. (or, in the alternative, Patel et al. in view of Li) and further in view of Iversen et al.

I. Patel et al. discloses all the limitations of the claim including the power module comprising carrier 502 and converter 518 (col.5: 4-6), the power module disclosed as capable of DC-to-DC conversion or AC-to-DC conversion (col.1: 11-16). Patel et al. further discloses that the power module disclosed provides reduced parasitic inductance and resistance in high frequency and high current applications (col.2: 49-60).

II. Patel et al. does not teach a DC-to-AC inverter.

III. Iversen et al. discloses a power delivery system that, among other things, provides reduced parasitic inductance and resistance in high frequency and high current applications (col.1: 47-56; col.4: 3-6), wherein the power delivery system may be any one of AC-to-AC and DC-to-DC converters, AC-to-DC rectifiers and DC-to-AC inverters (col.3: 47-54), depending on the requirements of the application.

IV. Since both Patel et al. and Iversen et al. both teach power delivery systems to a variety of high frequency and high current electrical and electronic applications, then the use of a DC-to-AC inverter power delivery system, taught by Iversen et al., for an application requiring AC power from a DC source would have been readily recognized in the power delivery system of the pertinent art of Patel et al.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the power module of Patel et al. so that it delivers power as a DC-to-AC inverter for applications requiring AC power from a DC source, as taught by Iversen et al.

6. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Patel et al. (or, in the alternative, Patel et al. in view of Li) and further in view of McDonnal.

I. Patel et al. discloses all the limitations of the claim and further teaches a power module package, i.e., a DC-to-DC converter comprising the carrier 502 and the SDC 518 mounted thereon (Fig. 5; col.1: 11-13 and 21-24; col.3: 31-35).

II. Patel et al. does not teach that the signal modifying circuit--input capacitor 522 and input inductor 524 (col.3: 63-64 and col.5: 14-15)--comprises an overvoltage protection device.

III. McDonnal discloses a DC-to-DC converter (Fig. 1) comprising an overvoltage protection device (circuit 80; col.4: 20-23) for the purpose of protecting the electrical system and the converter that provides the system power.

IV. Since McDonnal and Patel et al. both teach DC-to-DC converters for providing DC power to an electrical system, then an overvoltage circuit incorporated into

the DC-to-DC converter, as taught by McDonnal, would have been readily recognized in the pertinent art of Patel et al. as a vital feature ensuring the reliability and safety of the DC-to-DC converter and electronic system to which the converter supplies the DC power.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate an overvoltage circuit in the power module package (i.e., the DC-to-DC converter) of Patel et al., as taught by McDonnal, in order to ensure the reliability and safety of the electronic system on adapter 506 and user circuit board 516 of Patel et al.

Allowable Subject Matter

7. Claim 16 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter:

As to Claim 16, patentability resides in *a signal modifying circuit between the first interconnect on the second surface and the second interconnect on the second surface*, in combination with the other limitations of the claim.

Respons to Argum nts

9. Applicant's arguments filed August 11, 2003 have been fully considered but they are not persuasive.

(i) The Applicant disagrees with the Examiner's interpretation of "intended use" in the 35 USC § 102(e) rejection of Claim 1 over Patel et al. The Examiner holds his position as stated in the rejection because the phrase "comprising a through hole interconnect" in the limitation "the at least one second interconnect comprising a through hole connect" claimed by the Applicant, and supported in the Applicant's disclosure (interconnect 108 in Figs. 3 and 4, and p.7, lines 15-21 of the Specification), is nothing more than an indication that the second interconnect has a structure intended for as use as being connected to a another structure having a through hole, e.g., a printed circuit board. Again, **neither** a pin-receiving socket structure **nor** a through hole structure (e.g., a printed circuit board) is positively claimed as a structural feature of Claim 1 by the Applicant, and therefore **neither** socket **nor** through hole structure is required to be met by the prior art. The package pin 508 of Patel et al. is sufficient to read on the limitation of "at least one second interconnect comprising a through hole connect," as claimed in Applicant's Claim 1, since "through hole connects" are pins (as taught in Applicant's disclosure) and Patel et al. teaches pins 508 on the adapter 506. It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art

apparatus satisfying the claimed structural limitations. *Ex parte Masham*, 2 USPQ2d 1647 (1987).

(ii) The Applicant believes that Patel et al. in view of Li do not suggest that the reduction in signal noise due to parasitic inductance introduced by pin sockets. While Li is silent as to this feature, Li does, nevertheless, show that eliminating the socket and directly connecting the pins of the package to through holes of the circuit board is an art-recognized equivalent to using pin sockets, as indicated in the 35 USC § 103(a) rejection of Claim 1, above. The Examiner still believes that removing the pin socket *reduces the conductive path length* between the package and the printed circuit board, hence, *reduces parasitic inductance* which becomes significant at higher signal frequencies. However, without conceding to Applicant's position, the Examiner has nevertheless set aside the "*parastic inductance*" position in favor of a more structural rationale (set forth in the rejection, above) that would have been readily recognized in the pertinent art of Patel et al. by one of ordinary skill in the art as sound motivation for modifying Patel et al. by removing the socket and connecting the adapter pins directly to the through holes of the printed circuit board, as taught by Li. This reasoning, in combination with the explicit showing by Li of art-recognized equivalence between *pin sockets* and *direct-connection circuit-board-fabricated through holes* as alternative coupling structures for connecting the adapter pin interconnects to the circuit board strongly makes the case for obviousness over Patel et al. in view of Li. The Examiner further points out that, as indicated in the first paragraph of MPEP § 2144, "[t]he rationale to modify or combine the prior art does not have to be expressly stated in the

prior art; the rationale may be expressly or impliedly contained in the prior art or it may be reasoned from knowledge generally available to one of ordinary skill in the art, established scientific principles, or legal precedent established by case law."

(iii) In view of (i) and (ii) above, the rejections of the previous Office Action have been repeated with some minor editorial changes, and omission and modification of rationale, in sections III, IV and V under section 3, Rejection #2 of Claim 1 (pp.4-7 of the present Office Action) based on the same prior art and structure disclosed therein for reinforcement and enhancement of the Examiner's original rejection position of the previous Office Action of March 6, 2003 in said sections III, IV and V.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Smith et al. (US 5,694,297) discloses a package 300 with through hole connects (pins) 304 for connection with the pin holes of a socket (not shown) or a printed circuit board (Fig. 4; col.6: 66-col.7: 2).

Porter et al. (US 5,923,176) discloses a high-speed test fixture directly attached to the solder side of the PCB that carries the chip under test in order to eliminate the need for an adapter pin socket which lengthens the conductive path for the signal and consequently introduces parasitic signal path inductances that cause circuit noise (Abstract; col.1: 25-28).

Lawrence (US 3,719,860) teaches mounting a chip to a board without using pin sockets, disclosing that, among the disadvantages of using such sockets, are that they add weight and complexity to the board and are susceptible to mechanical shock and vibrations that may loosen a component or cause circuit noise (col.1: 54-59).

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 703-308-1205 (Crystal City campus) and 571-272-1936 (Carlyle campus). The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo, can be reached on 703-308-1233 (Crystal City campus) and 571-272-1957 (Carlyle campus). The fax phone numbers for the organization

where this application or proceeding is assigned are 703-308-7382 for regular communications and 703-308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

John B. Vigushin
Examiner
Art Unit 2827

jbv
December 5, 2003